

400mA LOAD SWITCH FEATURING PRE-BIASED PNP TRANSISTOR AND ESD PROTECTED N-MOSFET
Features

- Voltage Controlled Small Signal Switch
- N-MOSFET with ESD Gate Protection
- Ideally Suited for Automated Assembly Processes
- **Lead Free By Design/ROHS Compliant (Note 1)**
- **"Green" Device (Note 2)**

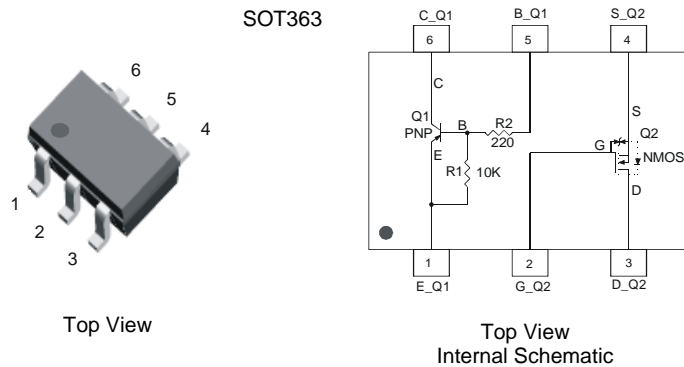
Description

LMN400E01 is best suited for applications where the load needs to be turned on and off using control circuits like micro-controllers, comparators etc. particularly at a point of load. It features a discrete pass transistor with stable $V_{CE(SAT)}$ which does not depend on input voltage and can support continuous maximum current of 400 mA. It also contains an ESD protected discrete N-MOSFET that can be used as control. The component can be used as a part of a circuit or as a stand alone discrete device.

Mechanical Data

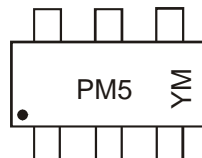
- Case: SOT363
- Case Material: Molded Plastic. "Green Molding" Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020C
- Terminal Connections: See Diagram
- Terminals: Finish - Matte Tin annealed over Alloy 42 leadframe. Solderable per MIL-STD-202, Method 208
- Marking Information: See Page 8
- Ordering Information: See Page 8
- Weight: 0.006 grams (approximate)

Reference	Device Type	R1(NOM)	R2(NOM)	Figure
Q1	PNP Transistor	10K	220	2
Q2	N-MOSFET	—	—	2


Ordering Information (Note 3)

Device	Packaging	Shipping
LMN400E01-7	SOT363	3000/Tape & Reel

- Notes:
1. No purposefully added lead.
 2. Diodes Inc.'s "Green" policy can be found on our website at <http://www.diodes.com>.
 3. For packaging details, go to our website at <http://www.diodes.com>.

Marking Information


PM5 = Product Type Marking Code,
 YM = Date Code Marking
 Y = Year, e.g., Y = 2011
 M = Month, e.g., 9 = September

Date Code Key

Year	2006	2007	2008	2009	2010	2011	2012	2013				
Code	T	U	V	W	X	Y	Z	A				
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings, Total Device @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 4)	P_D	200	mW
Power Derating Factor above 37.5°C	P_{der}	1.6	mW/ $^\circ\text{C}$
Output Current	I_{out}	400	mA

Thermal Characteristics @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic	Symbol	Value	Unit
Operating and Storage Temperature Range	T_j, T_{STG}	-55 to +150	$^\circ\text{C}$
Thermal Resistance, Junction to Ambient Air (Note 4)	$R_{\theta JA}$	625	$^\circ\text{C/W}$

**Maximum Ratings:
Pre-Biased PNP Transistor (Q1)** @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	-50	V
Collector-Emitter Voltage	V_{CEO}	-50	V
Supply Voltage	V_{CC}	-50	V
Input Voltage	V_{in}	-6 to +5	V
Output Current	I_C	-400	mA

**Maximum Ratings:
ESD Protected N-Channel MOSFET (Q2)** @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	60	V
Drain Gate Voltage ($R_{GS} \leq 1\text{M Ohm}$)	V_{DGR}	60	V
Gate-Source Voltage	V_{GSS}	Continuous	+/-20
		Pulsed ($t_p < 50 \mu\text{S}$)	+/-40
Drain Current (Note 4)	I_D	Continuous ($V_{GS} = 10\text{V}$)	300
		Pulsed ($t_p < 10 \mu\text{S}$, Duty Cycle <1%)	800
Continuous Source Current	I_S	300	mA

Notes: 4. Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch; pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at <http://www.diodes.com/datasheets/ap02001.pdf>.

Electrical Characteristics: Pre-Biased PNP Transistor (Q1) @T_A = 25°C unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 5)						
Collector-Base Cut Off Current	I _{CBO}	—	—	-500	nA	V _{CB} = -50V, I _E = 0
Collector-Emitter Cut Off Current	I _{CEO}	—	—	-1	uA	V _{CE} = -50V, I _B = 0
Collector-Base Breakdown Voltage	V _{(BR)CBO}	-50	—	—	V	I _C = -10uA, I _E = 0
Collector-Emitter Breakdown Voltage	V _{(BR)CEO}	-50	—	—	V	I _C = -2mA, I _B = 0
Input Off Voltage	V _{I(OFF)}	-0.3	-0.55	—	V	V _{CE} = -5V, I _C = -100uA
Output Current	I _{O(OFF)}	—	—	-1	uA	V _{CC} = -50V, V _I = 0V
ON CHARACTERISTICS (Note 5)						
Collector-Emitter Saturation Voltage	V _{CE(SAT)}	—	—	-0.15	V	I _C = -10mA, I _B = -0.3mA
		—	—	-0.3	V	I _C = -200mA, I _B = -20mA
		—	—	-0.5	V	I _C = -400mA, I _B = -40mA
		—	—	-0.6	V	I _C = -500mA, I _B = -50mA
DC Current Gain	h _{FE}	55	220	—	—	V _{CE} = -5V, I _C = -50mA
		55	225	—	—	V _{CE} = -5V, I _C = -400mA
Input On Voltage	V _{I(ON)}	-3	-1.5	—	V	V _O = -0.3V, I _C = -20mA
Output Voltage (Equivalent to V _{CE(SAT)})	V _{O(ON)}	—	-0.1	-0.3	V	I _O /I _I = -50mA / -2.5mA
Input Current	I _I	—	-18	-45	mA	V _I = -5V
Base-Emitter Turn-on Voltage	V _{BE(ON)}	—	-1.2	-1.6	V	V _{CE} = -5V, I _C = -400mA
Base-Emitter Saturation Voltage	V _{BE(SAT)}	—	-1.9	-2.5	V	I _C = -50mA, I _B = -5mA
Input Resistor (Base), +/- 30%	R2	0.154	0.22	0.286	KΩ	—
Pull-up Resistor (Base to V _{CC} supply), +/- 30%	R1	7	10	13	KΩ	—
Resistor Ratio (Input Resistor/Pullup resistor)	R1/R2	36	45	55	—	—
SMALL SIGNAL CHARACTERISTICS						
Gain Bandwidth Product	f _T	—	200	—	MHz	V _{CE} = -10V, I _E = -5mA, f = 100MHz

Notes: 5. Short duration pulse test used to minimize self-heating effect.

Electrical Characteristics:
ESD Protected N-Channel MOSFET (Q2) @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 5)						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	60	—	—	V	$V_{GS} = 0V, I_D = 10\mu A$
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	μA	$V_{GS} = 0V, V_{DS} = 60V$
Gate-Body Leakage Current, Forward	I_{GSSF}	—	—	10	μA	$V_{GS} = 20V, V_{DS} = 0V$
Gate-Body Leakage Current, Reverse	I_{GSSR}	—	—	-10	μA	$V_{GS} = -20V, V_{DS} = 0V$
ON CHARACTERISTICS (Note 5)						
Gate Source Threshold Voltage	$V_{GS(th)}$	1	1.6	2.5	V	$V_{DS} = V_{GS}, I_D = 0.25mA$
Static Drain-Source On-State Voltage	$V_{DS(on)}$	—	0.09	1.9	V	$V_{GS} = 5V, I_D = 50mA$
		—	0.6	3.75		$V_{GS} = 10V, I_D = 500mA$
On-State Drain Current	$I_{D(on)}$	500	—	—	mA	$V_{GS} = 10V,$ $V_{DS} \geq 2 * V_{DS(ON)}$
Static Drain-Source On Resistance	$R_{DS(on)}$	—	1.6	3	Ω	$V_{GS} = 5V, I_D = 50mA$
		—	1.2	2		$V_{GS} = 10V, I_D = 500mA$
Forward Transconductance	g_{FS}	80	260	—	mS	$V_{DS} \geq 2 * V_{DS(ON)}, I_D = 200 mA$
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{iss}	—	—	50	pF	$V_{DS} = -25V, V_{GS} = 0V, f = 1MHz$
Output Capacitance	C_{oss}	—	—	25	pF	
Reverse Transfer Capacitance	C_{rss}	—	—	5	pF	
SWITCHING CHARACTERISTICS (Note 5)						
Turn-On Delay Time	$t_{d(on)}$	—	—	20	ns	$V_{DD} = 30V, V_{GS} = 10V,$ $I_D = 200mA,$ $R_G = 25 \text{ Ohm}, R_L = 150 \text{ Ohm}$
Turn-Off Delay Time	$t_{d(off)}$	—	—	40	ns	
SOURCE-DRAIN (BODY) DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
Drain-Source Diode Forward On-Voltage	V_{SD}	—	0.88	1.5	V	$V_{GS} = 0V, I_S = 300 mA^*$
Maximum Continuous Drain-Source Diode Forward Current (Reverse Drain Current)	I_S	—	—	300	mA	
Maximum Pulsed Drain-Source Diode Forward Current	I_{SM}	—	—	800	mA	

Notes: 5. Short duration pulse test used to minimize self-heating effect.

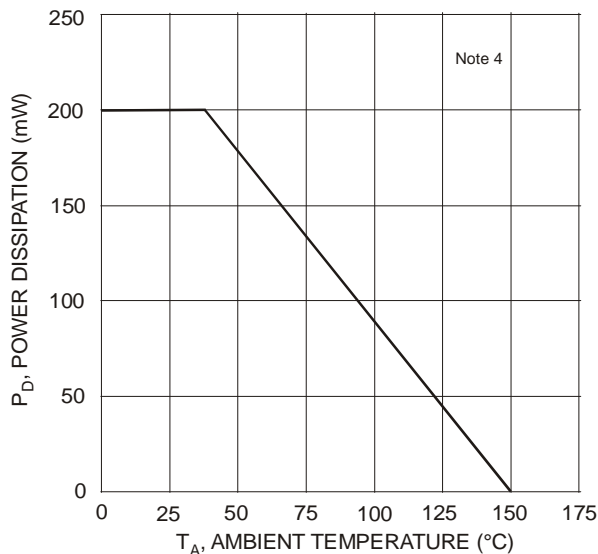


Fig. 3 Max Power Dissipation vs. Ambient Temperature

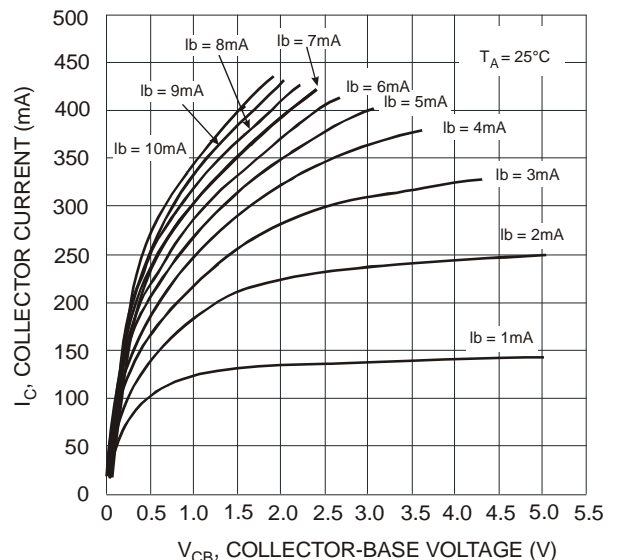


Fig. 4 Output Current vs. Voltage Drop (Pass Element PNP)

Pre-Biased PNP Transistor Characteristics

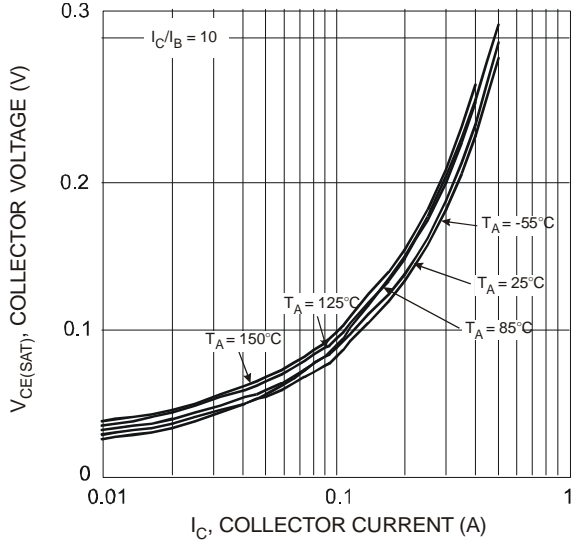


Fig. 5 $V_{CE(SAT)}$ vs. I_C @ $I_C/I_B = 10$

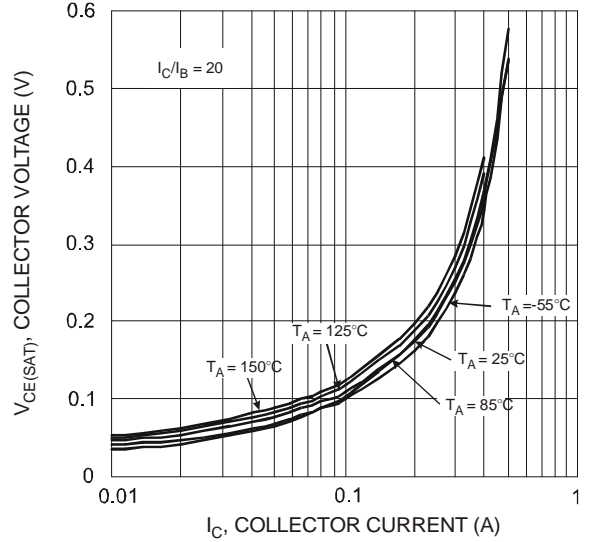


Fig. 6 $V_{CE(SAT)}$ vs. I_C @ $I_C/I_B = 20$

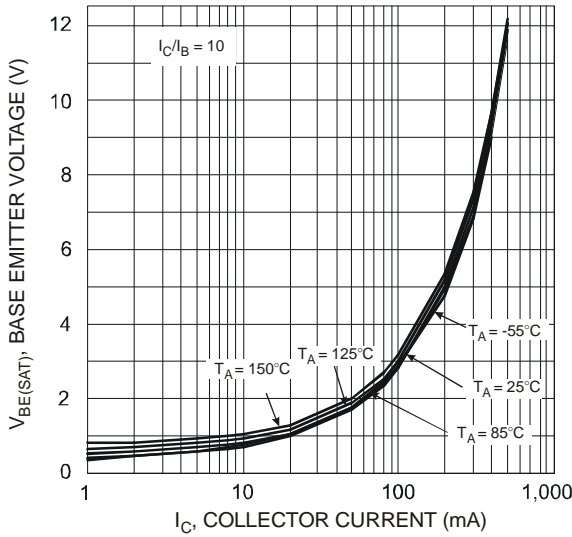


Fig. 7 $V_{BE(SAT)}$ vs. I_C @ $I_C/I_B = 10$

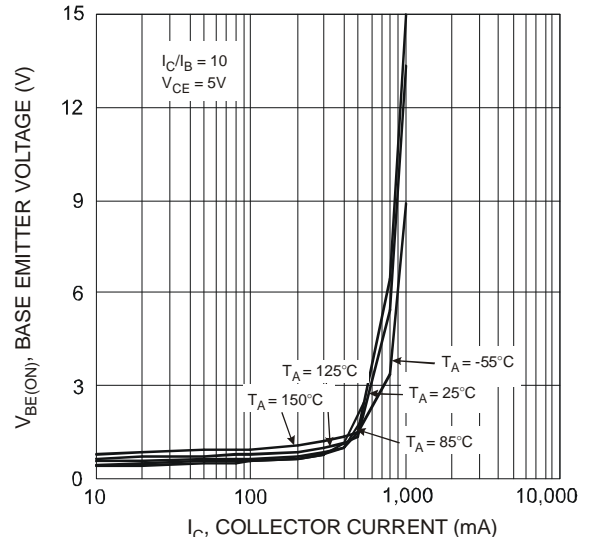


Fig. 8 $V_{BE(ON)}$ vs. I_C @ $V_{CE} = 5\text{V}$

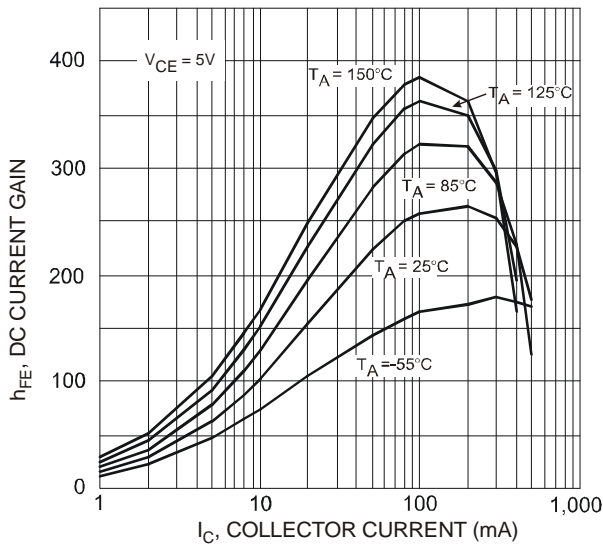


Fig. 9 h_{FE} vs. I_C @ $V_{CE} = 5\text{V}$

Typical N-Channel MOSFET (ESD Protected) Characteristics

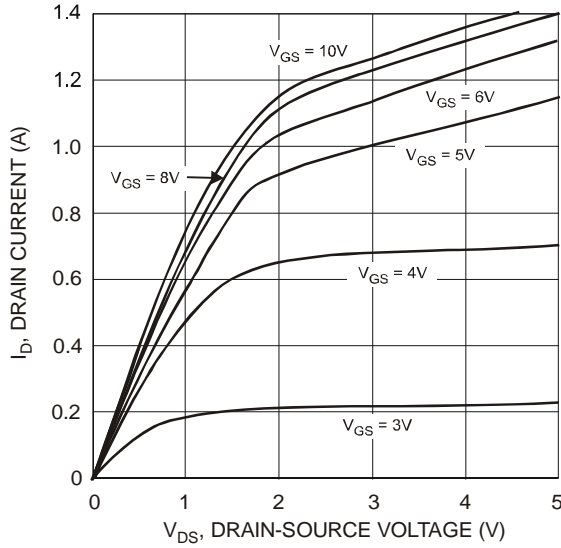


Fig. 10 Output Characteristics

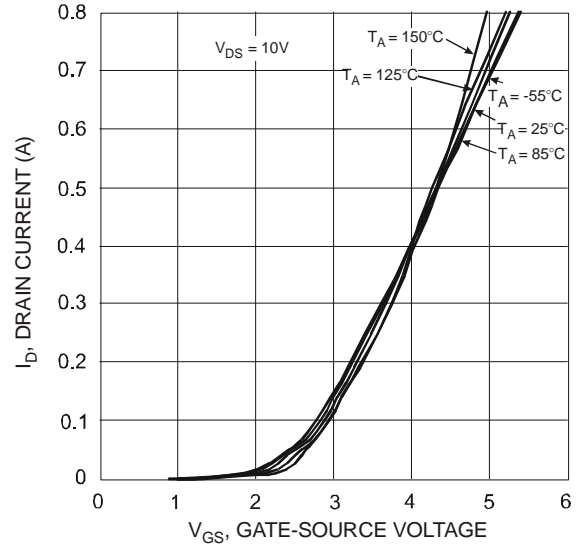


Fig. 11 Transfer Characteristics

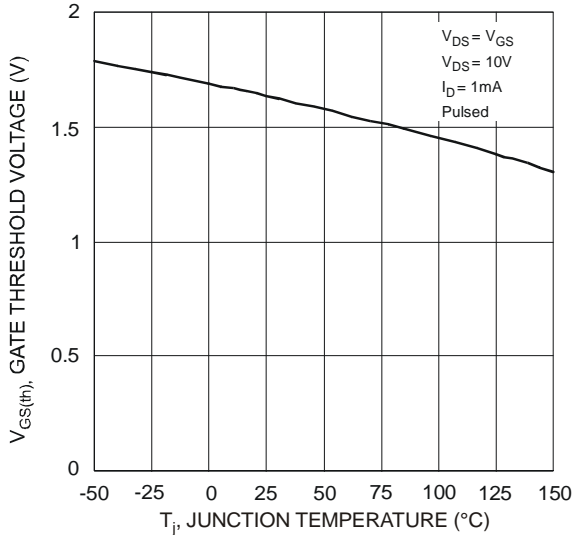


Fig. 12 Gate Threshold Voltage vs. Junction Temperature

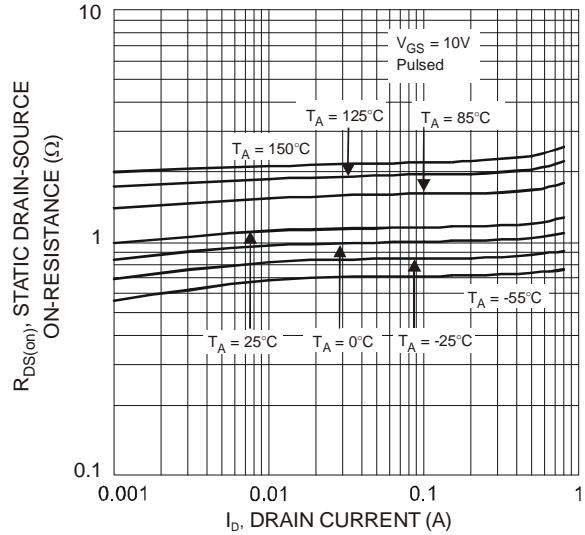


Fig. 13 Static Drain-Source On-Resistance vs. Drain Current

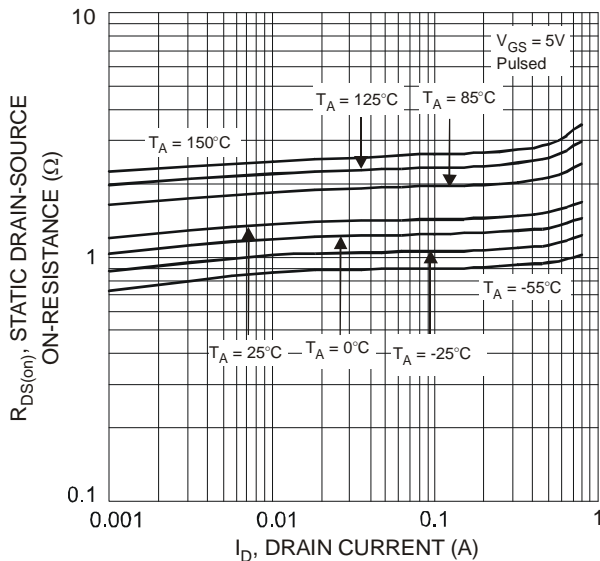


Fig. 14 Static Drain-Source On-Resistance vs. Drain Current

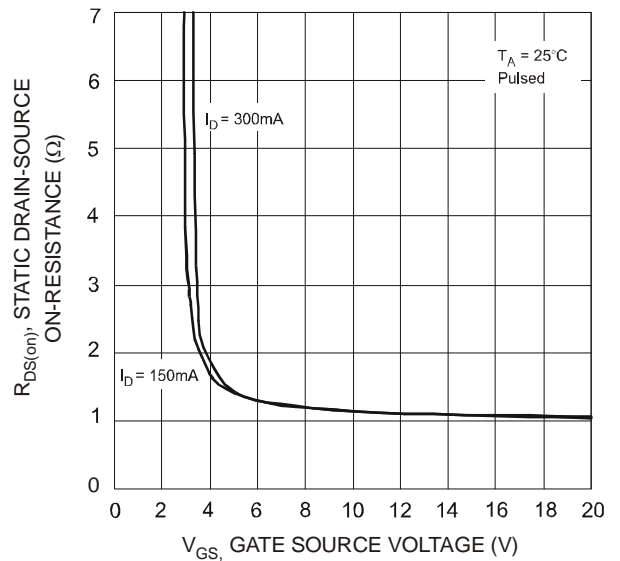


Fig. 15 Static Drain-Source On-Resistance vs. Gate-Source Voltage

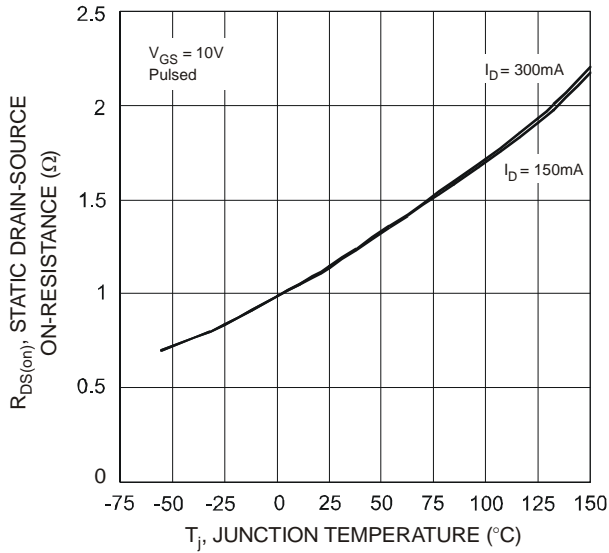


Fig. 16 Static Drain-Source On-State Resistance vs. Junction Temperature

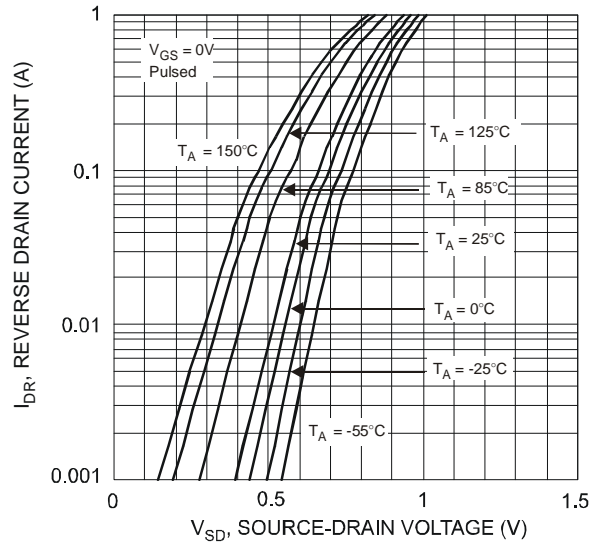


Fig. 17 Reverse Drain Current vs. Source-Drain Voltage

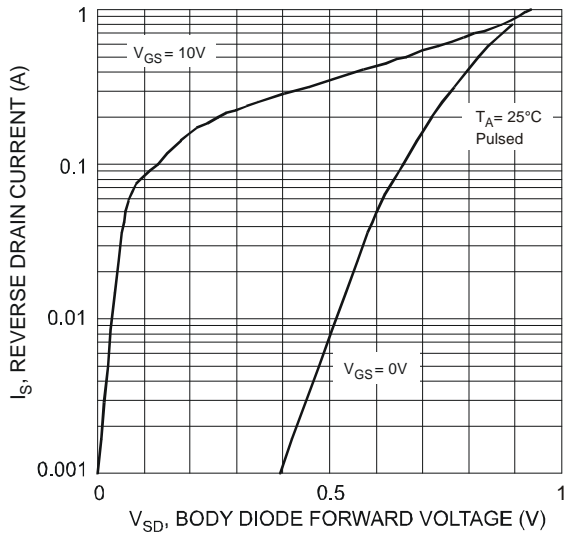


Fig. 18 Reverse Drain Current vs. Source-Drain Voltage

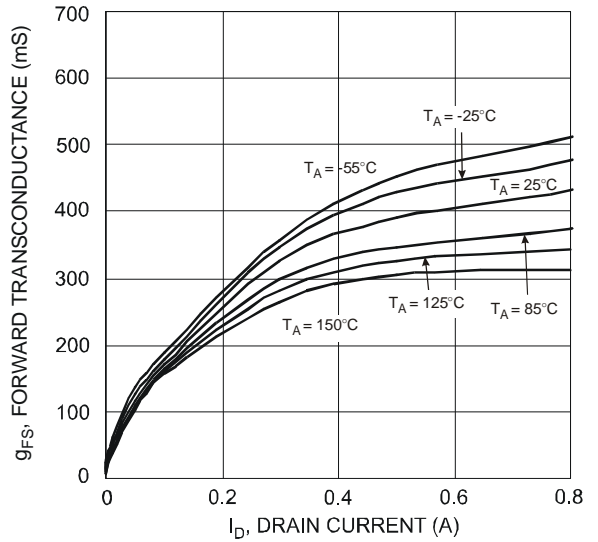


Fig. 19 Forward Transconductance vs. Drain Current ($V_{DS} > I_D * R_{DS(ON)}$)

Application Details

PNP Transistor and ESD Protected N-MOSFET integrated as one in LMN400E01 can be used as a discrete entity for general application or as an integrated circuit to function as a Load Switch. When it is used as the latter as shown in Fig. 20, various input voltage sources can be used as long as it does not exceed the maximum ratings of the device. These devices are designed to deliver continuous output load current up to a maximum of 400 mA. The MOSFET Switch draws no current, hence loading of control circuitry is prevented. Care must be taken for higher levels of dissipation while designing for higher load conditions. These devices provide high power and also consume less space. The product mainly helps in optimizing power usage, thereby conserving battery life in a controlled load system like portable battery powered applications. (Please see Fig. 21 for one example of a typical application circuit used in conjunction with a voltage regulator as a part of power management system).

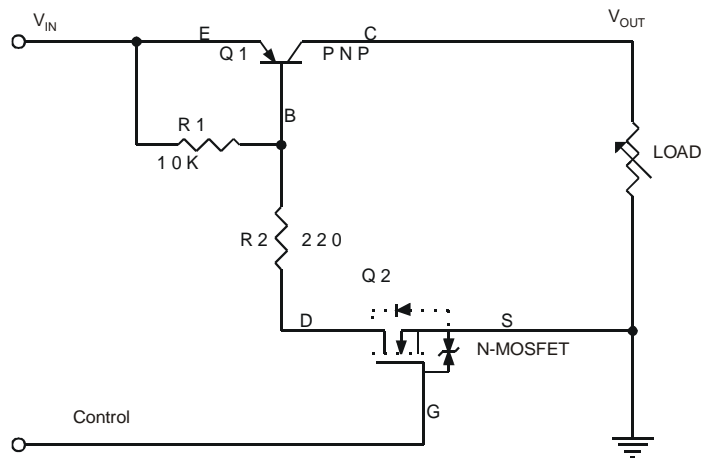


Fig. 20 Circuit Diagram

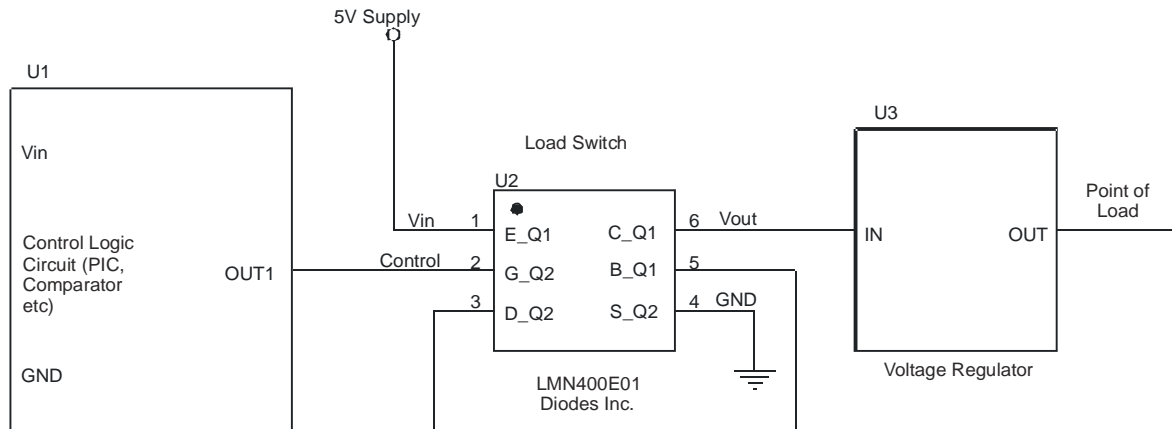
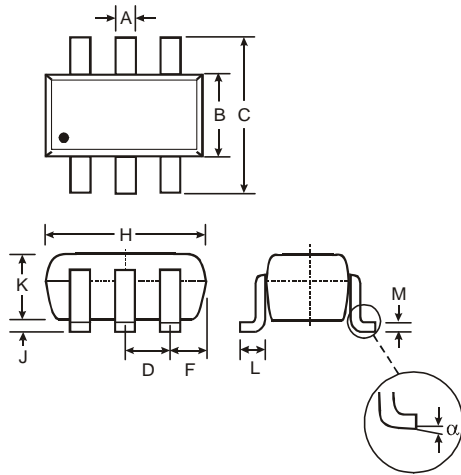


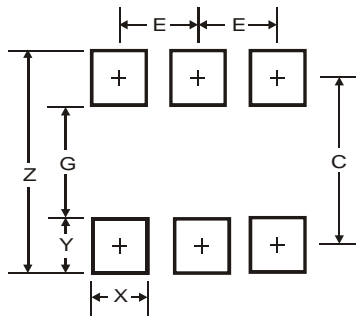
Fig. 21 Typical Application Circuit

Package Outline Dimensions



SOT-363		
Dim	Min	Max
A	0.10	0.30
B	1.15	1.35
C	2.00	2.20
D	0.65 Nominal	
F	0.30	0.40
H	1.80	2.20
J	-	0.10
K	0.90	1.00
L	0.25	0.40
M	0.10	0.25
α	0°	8°
All Dimensions in mm		

Suggested Pad Layout



Dimensions	Value (mm)
Z	2.5
G	1.3
X	0.42
Y	0.6
C	1.9
E	0.65

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